Substitute for Form 1449 A & B/PTO			Complete if Known	
			Application Number	Cont. of Serial No. 09/425,886
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Confirmation Number	Not Yet Assigned
			Filing Date	June 24, 2003
			First Named Inventor	Pranav ASHAR et al.
			Art Unit	Not Yet Assigned 2133
			Examiner Name	Not Yet Assigned ABRAHAM
Sheet	2	of	2	Attorney Docket Number	A8612

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Examiner Initials*	Cite No.[1]	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		Number	Kind Code[2] (if known)		

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Examiner Initials*	Cite No.[1]	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Translation[6]
		Country Code[3]	Number[4]	Kind Code[5] (if known)			

OTHER ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation[6]
EA		SENTOVICH, E., et al. "Sequential Circuit Design Using Synthesis and Optimization", Proceedings of ICCD, 1992	
EA		GUPTA, A., ASHAR, P., "Integrating a Boolean Satisfiability and BDDS for Combinational Verification, Proceedings of VLSI Design 98, pp. 222-225, 1998	
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Examiner Signature	Esaw Abraham	Date Considered	06/24/04

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[1]Applicant's unique citation designation number (optional). [2]See Kind Codes of USPTO Patent Documents at www.uspto.gov, MPEP 901.04 or in the comment box of this document. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to indicate here if English language Translation is attached.

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Sheet	1	of	2	Attorney Docket Number	A8612

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EA		ABADIR, M., FERGUSON, J., KIRKLAND, Thomas E. "Logic Design Verification via Test Generation"; IEEE Translations on Computer Aided Design, vol. 7, no. 1, pp. 138-148, January 1988	
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